Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **INPUT**
2. **OUTPUT**
3. **GND**

**.074”**

**3**

**2**

**1**

**MASK**

**REF**

**CE7808**

**.080”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size = .010 x .022”**

**Backside Potential: GND**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .076” X .081” DATE: 10/1/19**

**MFG: SILICON GENERAL THICKNESS .014” P/N: SG7808**

**DG 10.1.2**

#### Rev B, 7/1